SWCNT-MoS₂-SWCNT Vertical Point Heterostructures

Jin Zhang, Yang Wei,* Fengrui Yao, Dongqi Li, He Ma, Peng Lei, Hehai Fang, Xiaoyang Xiao, Zhixing Lu, Juehan Yang, Jingbo Li, Liying Jiao, Weida Hu, Kaihui Liu, Kai Liu, Peng Liu, Qunqing Li, Wei Lu, Shoushan Fan, and Kaili Jiang*

Two-dimensional (2D) semiconducting materials, such as transition metal dichalcogenides (TMDCs), have attracted intense attention due to their excellent electronic and optoelectronic properties.[1–3] A variety of van der Waals (vdW) heterostructures can be further made by layer-by-layer stacking of 2D nanomaterials,[4–8] 2D nanomaterials and single-walled carbon nanotube (SWCNT) films[9] as well as 2D–3D materials.[10,11] Such vertically stacked heterostructures have shown unique properties[12] and have great potentials in nanoelectronics,[13–15] flexible electronics,[16,17] optoelectronics,[18–21] etc. Although these stacked 2D heterostructures possess nanoscaled vertical dimension, their in-plane sizes are usually in microscale. Therefore,

J. Zhang, Prof. Y. Wei, D. Li, Dr. H. Ma, P. Lei, X. Xiao,
Prof. P. Liu, Prof. Q. Li, Prof. S. Fan, Prof. K. Jiang
State Key Laboratory of
Low-Dimensional Quantum Physics
Department of Physics and Tsinghua-Foxconn
Nanotechnology Research Center
Tsinghua University
Beijing 100084, China
E-mail: WeiYang@tsinghua.edu.cn; JiangKL@tsinghua.edu.cn
F. Yao, Prof. K. H. Liu
State Key Laboratory for Mesoscopic Physics
School of Physics
Peking University
Beijing 100871, China
H. Fang, Prof. W. Hu, Prof. W. Lu
National Laboratory for Infrared Physics
Shanghai Institute of Technical Physics
Chinese Academy of Sciences
500 Yu Tian Road, Shanghai 200083, China
Z. Lu, Prof. L. Jiao
Key Laboratory of Organic Optoelectronics
and Molecular Engineering of the Ministry of Education
Department of Chemistry
Tsinghua University
Beijing 100084, China
J. Yang, Prof. J. Li
State Key Laboratory for Superlattice and Microstructures
Institute of Semiconductors
Chinese Academy of Sciences
Beijing 100083, China
Prof. K. Liu
State Key Laboratory of New Ceramics and Fine Processing
School of Materials Science and Engineering
Tsinghua University
Beijing 100084, China
Prof. Q. Li, Prof. S. Fan, Prof. K. Jiang
Collaborative Innovation Center of Quantum Matter
Beijing 100084, China

scaling down the vdW heterostructures into nanoscale is an essential issue for the practical applications, as smaller device will have lower power consumption and higher spatial resolution. The top-down methodology is a feasible solution, but it will encounter problems when the devices are small to a certain extent. For example, graphene can be employed as electrodes in the vdW heterostructures, but the bandgap will be opened if graphene is tailored into a nanoribbon.[22,23] Moreover, with decreasing width of the 2D nanoribbons the proportion of the edge atoms increases. The effects induced by the defects and adsorbates at the edge cannot be neglected any more. Consequently, constructing 2D heterostructures in nanoscale is still a challenge. On the other hand, SWCNTs are perfect 1D atomic crystals, which have atomic smooth surface, nanoscaled diameters, and superior electronic properties.[24,25] It is thus possible to construct a 1D–2D hybrid vertical structure with individual SWCNT and 2D atomic crystal. The functional area of such devices can be well defined within nanoscale without nanolithography, thanks to the introduction of the SWCNTs.

Here, a crossed structure is employed to construct an SWCNT-MoS₂-SWCNT vertical point heterostructure (VPH), in which a piece of 2D MoS₂ is sandwiched by two cross-stacked metallic SWCNTs.[26] The overlapped area is defined by the diameters of the SWCNTs, which are in the range of 1–2 nm. This feature size can hardly be achieved by conventional microfabrication techniques. Experimental results indicate that the on/off ratio of the VPH field effect transistor (FET) ranges from 10^5 to 10^6 at room temperature and the current density through the VPH can be as high as 10^7 A cm^{-2}. Furthermore, scanning photocurrent microscopy (SPCM) images reveal that the VPH can be applied as a light detector to plot a focused laser beam (≈1 μm), showing its ability in spatial resolution. The novel VPH facilely scales down the vertical 2D device by a bottom-up approach and the proof-of-principle devices have shown the possibility of fabricating 1D–2D hybrid structures for the future nanoelectronics and nanooptoelectronics.

The VPH is sketched in **Figure 1**a. A thin layer of MoS₂ is sandwiched between two cross-stacked metallic SWCNTs. The fabrication processes are illustrated in Figure S1 (Supporting Information). A layer of horizontally aligned SWCNTs was first transferred from quartz to silicon substrate with 300 nm silica via poly(methyl methacrylate) (PMMA)-assisted transfer technique.[27,28] A mechanically exfoliated MoS₂ layer was then transferred on the SWCNTs, followed by another SWCNT layer with alignment perpendicular to the first SWCNT layer. The VPHs with two metallic SWCNTs were efficiently identified by the type-dependent contrast of SWCNTs under scanning electron microscopy (SEM)[29,30] and further checked by electrical measurements (Figure S2, Supporting Information). Ti/Au

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Figure 1. Schematic illustration and morphology of VPH. a) A schematic illustration of VPH in the perspective view. b) Schematic illustration of VPH in the cross-sectional view and the wiring diagram. Gating voltage is applied between the bottom SWCNT and the p++ doped silicon. Source-drain bias is applied between top and bottom SWCNTs. c) A SEM image of the VPH. Inset is the corresponding optical image. Scale bar: 5 µm.

(5/50 nm) electrodes on the two metallic SWCNTs were fabricated by electron beam lithography, electron beam evaporation, and lift-off procedure. The VPH devices were then isolated from the SWCNT networks by oxygen plasma treatment. The samples were annealed at 350 °C in 400 mTorr Ar/H$_2$ for 30 min to improve contacts. Figure 1c shows a SEM image and corresponding optical microscopy image of an as-fabricated VPH. Atomic force microscopy (AFM) measurement indicates that the MoS$_2$ flake is 19 nm in thickness (Figure S3, Supporting Information), and the SWCNTs were ≈1 nm in diameter.

The electrical transport properties of the VPH were studied under vacuum at room temperature. **Figure 2**c shows the output characteristics with gate voltage being varied from −10 to 10 V in steps of 5 V. These results indicate that the current increases with increasing positive V_G and thus validate that

electrons are the majority carriers in the MoS$_2$. In addition, it is known that the work function of SWCNT is ≈4.7 eV and the electron affinity of MoS$_2$ is ≈4.45 eV.[31,32] Consequently, a band diagram shown in Figure 2b can be sketched and used to further interpreting the mechanism. The Schottky barrier between the two metallic SWCNTs is simplified to a rectangle potential barrier, as the MoS$_2$ channel is ultrashort and it is totally depleted.[16,33] Both metallic SWCNTs form Schottky barriers with MoS$_2$ and their heights can be tuned by the back-gate potential (Figure 2b). The Schottky barriers become higher for electrons at negative gate voltages (right panel of Figure 2b). The thermionic emission currents can be effectively cut off at small source-drain bias, which can be found from the output curves at negative gate voltages. On the contrary, the Schottky barriers are lowered for electrons at positive gate voltages
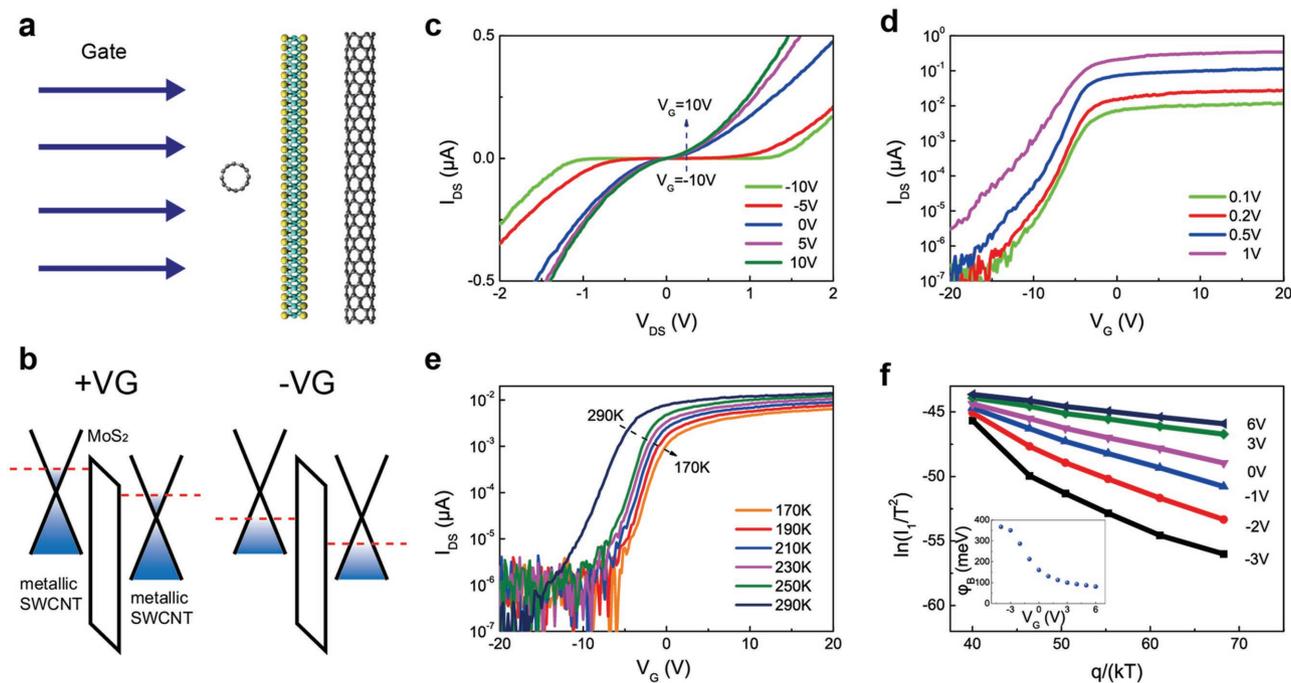
Figure 2. Band diagram and electrical transport characteristics of VPH. a) Schematic illustration of a VPH under gate electric. Gate electric field is applied from silicon back gate. b) Band diagram of biased VPH with negative and positive gate voltages. c) Output characteristics of the VPH FET at different gate voltages. Gate voltage varies from −10 to 10 V in steps of 5 V. d) Tranfer characteristic of the VPH FET at V_{DS} = 0.1, 0.2, 0.5, and 1 V. On/off ratios of the VPH FET exceed 10^5 at different V_{DS}. e) Tranfer characteristics of the VPH FET at different temperatures varying from 290 to 170 K (V_{DS} = 0.1 V). f) Temperature-dependent electrical transport characteristics at various gate voltages. Inset is the corresponding Schottky barrier heights derived from slopes of the plots in (f). V_G varies from −4 to 6 V with 1 V step variation.

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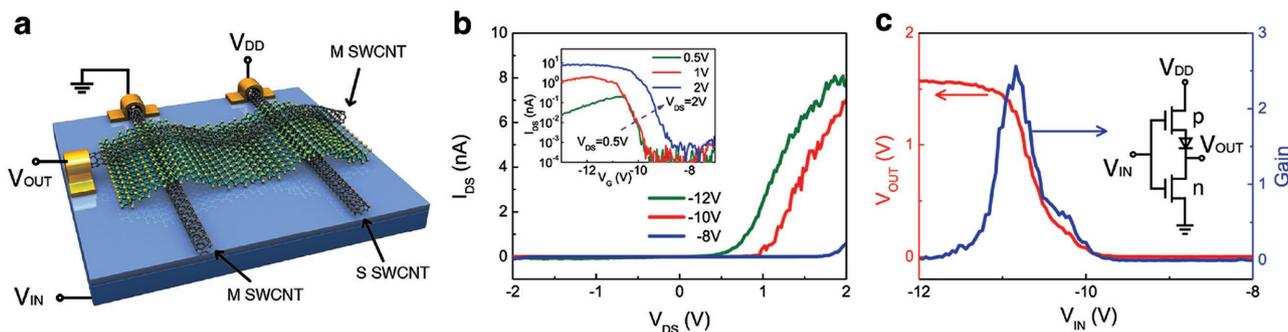
Figure 3. Complementary inverter with VPHs. a) Schematic diagram of the complementary inverter and the wiring diagram. b) Output characteristics of the pMOS at gate bias $V_G = -12$, -10, and -8 V. The bottom semiconducting SWCNT and top metallic SWCNT are drain and source, respectively. Inset is the corresponding transfer characteristics at $V_{DS} = 0.5$, 1, and 2 V. c) The complementary inverter characteristics. Inset is the equivalent circuit diagram of the inverter. A positive supply voltage ($V_{DD} = 2$ V) is applied to the semiconducting SWCNT and the gain is 2.6.

(left panel of Figure 2b) and the thermionic electrons can easily overcome the reduced Schottky barriers.

The transfer characteristics I_{DS} (V_G) is presented in Figure 2d. The bias was set at 0.1, 0.2, 0.5, and 1 V, respectively. The vertical transistor has high on/off ratio exceeding 10^5 at all these biases. It is extremely high compared with some recent reports.[13,14] The high on/off ratio can be ascribed to both the small effective function area of the VPH and negligible electric field screening induced by the bottom SWCNT. The sulfur vacancies in mechanically exfoliated MoS_2 can provide vertical conducting channels that cannot be effectively turned off by gate potential.[34] The extremely reduced in-plane size makes the VPH different. The diameters of SWCNTs are only about 1 nm and thus the function area is localized around the overlapping area about 1 nm^2. Therefore, the possibility of having defects locate within the function area is greatly reduced and the VPH can be effectively turned off. In addition, the vertical transistor has high on/off ratio no matter the V_{DS} is positive or negative. Moreover, such device can work very well even when the MoS_2 is three layers (Figure S4, Supporting Information), suggesting the robustness of the VPH.

More transport measurements were carried out at different temperatures to further study the mechanism. The temperature-dependent transfer characteristics are plotted in Figure 2e, where the bias (V_{DS}) is 0.1 V. These experimental results indicate that the current reduces with the decreasing temperature at the same V_G and V_{DS}. The physical picture is that the electrons have low kinetic energy at low temperature, thereby being blocked by the Schottky barrier. Furthermore, the thermionic-emission-diffusion theory can be used to analyze the results quantitatively. The current through VPH (I) can be expressed as[35]

$$I = AA^{**}T^2 \exp\left(-\frac{q\varphi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \quad (1)$$

where A is the conducting area, A^{**} is the effective Richardson constant, T is the temperature, q is elementary charge, φ_B is the Schottky barrier height, k is the Boltzmann constant, and V is the 0.1 V bias in this study. Conducting logarithm on both sides of Equation (1), we have $\ln(I_1/T^2) = \ln(AA^{**}) - q\varphi_B/kT$, where $I_1 = I/[\exp(qV/kT) - 1]$. The Schottky barrier heights at varied gate voltage can be determined by the slopes of $\ln(I_1/T^2) \sim q/kT$,

as shown in Figure 2f. The experimental plots approximately accord with linear relationship, indicating that the thermionic-emission-diffusion theory is applicable to the VPH device. The inset of Figure 2f shows that the Schottky barrier height derived from slopes of the plots can be modulated from 367 to 81 meV by varying V_G from -4 to 6 V, corresponding to turning on the FET. Note that there is a modest deviation from linearity in the case of high negative gate voltage and low temperature. The deviation can be attributed to emission currents contributed by the charge tunneling.[16,33]

The unique VPH can be potentially used as building blocks for complementary metal-oxide-semiconductor (CMOS) device. A facile CMOS was constructed by introducing an additional semiconducting SWCNT, as sketched in **Figure 3**a. The MoS_2 used in the CMOS is 39 nm in thickness. An equivalent circuit diagram can be found in the inset of Figure 3c. The left VPH is the nMOS. The pMOS is the p-doped SWCNT. They are connected together by the top metallic SWCNT (V_{out}) via the right VPH diode, a vertical p-n junction. Electric transport studies on the series structure consisted of the pMOS and the p-n junction revealed a typical rectifying characteristic at negative gating bias (Figure 3b). The calculated rectification ratios are about 10^2, 10^4, and 10 at -12, -10, and -8 V gate voltages, respectively. The series structure performs more like a rectifier diode as the p-doped SWCNT is turned on and the n-doped MoS_2 is not depleted when they are negatively gated properly. The series structure further shows a p-type transfer characteristic at forward bias 0.5, 1, and 2 V (inset of Figure 3b). The on current of the 0.5 V bias curve maximizes at a negative gate voltage, which is a little different to a conventional pMOS. It is due to the n-doped MoS_2 layer. As shown in Figure 2d, the MoS_2 channel can be turned off at large negative gate voltage and thus blocks the increase of electric currents at more negative gate voltage. Moreover, the VPH-based CMOS shows a typical complementary inverter characteristic with gain of about 2.6, as presented in Figure 3c.

The VPH can also be possibly applied for light detection with spatial resolution, since the device is localized around the overlapping area of the two cross SWCNTs. A strong response to light was first observed by monitoring the I_{DS} ($V_{DS} = 0.2$ V, $V_G = 0$ V) through the VPH during turning on and off the illumination light on the device from an optical microscope. Both the output characteristics and the time resolved I_{DS} show that

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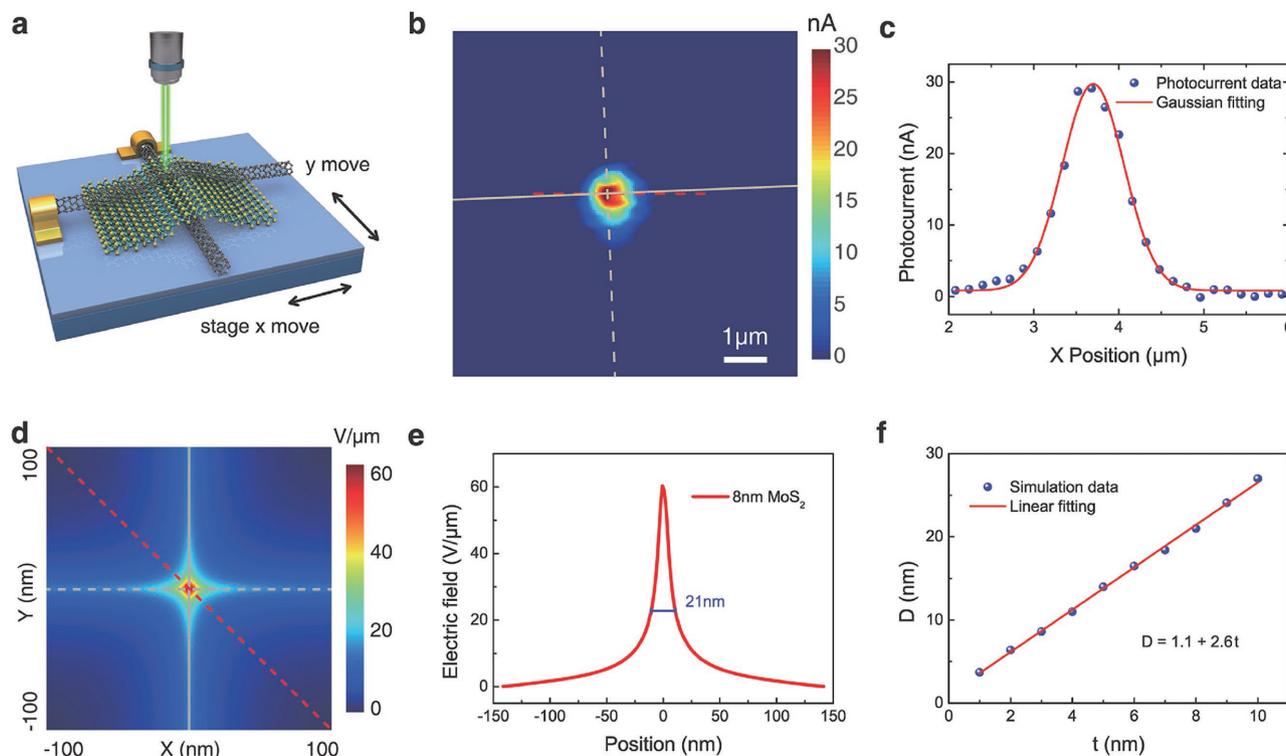
Figure 4. Scanning photocurrent mapping of VPH and corresponding electric field simulation. a) Schematic diagram of the SPCM. A 2D piezoelectric stage is used to drive the VPH to move around the focused laser. The photocurrents and positions are recorded, simultaneously. b) A SPCM image of a VPH at $V_{DS} = 0.1$ V. Thickness of the MoS$_2$ is 8 nm and scale bar is 1 μm. The horizontal and vertical gray lines stand for the two SWCNTs in the VPH. c) Gauss fitting of the photocurrents extracted from red dashed line in (b). Full width at half maximum derived from the fitting curve is 0.73 μm. d) Electric field simulation of VPH with 8 nm MoS$_2$. e) Electric field strength distribution along the red dashed diagonal line in (d). Width at the $1/e$ of maximum is 21 nm. f) Feature size versus the thickness of MoS$_2$.

the VPH device is sensitive to the visible light (Figure S5, Supporting Information). An SPCM was used to further study the VPH (**Figure** 4a). As some of the reported MoS$_2$ light detector is sensitive to the light with wavelength < ≈700 nm,[36,37] a 532 nm laser beam was thus employed to focus on the VPH through a 100× objective lens with numerical aperture of 0.95. A 2D piezoelectric stage was used to drive the VPH to move around the focused laser. SPCM images were mapped out by recording the photocurrents and positions, simultaneously. Figure 4b is such an image of a VPH with an 8 nm MoS$_2$ flake (Figure S6a, Supporting Information), under 0.1 V source–drain bias and 0.5 mW laser power. This image indicates a micrometer-sized spot around the VPH. Further studies (Figure 4c) show that the radial distribution curve of photocurrents (red dashed line) follows a typical Gaussian distribution, and the full width at half maximum (FWHM) is 0.73 μm. A similar scan photocurrent image with a 0.71 μm FWHM (Figure S6, Supporting Information) can be achieved under 0.2 V bias. Both agree well with the spot size of the focused laser beam. The photoresponsivity of the VPH can thus be calculated from these experimental results and it is ≈38 A W^{-1} at 0.1 V bias. Moreover, a conservative estimate on the spatial resolution of the VPH should be less than 0.16 μm, since SPCM image can discriminate the neighboring spots with a 0.16 μm step as shown in Figure 4c. According to these results and the fact that the VPH is much smaller than the laser spot, it is reasonable to conclude that the VPH light detectors have the ability to map the spot of the focused laser beam and have potential in light detection with high spatial resolution.

The performance on spatial resolution of VPH light detector can be ascribed to the localized electric field. Electric field simulation (Figure 4d) shows the electric field strength distribution of such a 1 V-biased VPH with 8 nm thick MoS$_2$, indicating that the electric field is localized around the cross point. Here we define the width at 1/e of maximum electric field along the red dashed diagonal line (Figure 4e) as a feature size, named as D. The feature size is about 21 nm in Figure 4d. The thickness-dependent feature sizes are plotted in Figure 4f, indicating a linear dependence $D = 1.1 + 2.6\,t$, where t is the thickness of 2D nanomaterials. The photocurrents are mainly generated within the region of intense localized electric field where electrons and holes are effectively separated. Therefore, it is reasonable that the VPH light detectors have high spatial resolution, which will be further revealed by the antenna-enhanced photocurrent measurement and near field optics methodology.[38]

In conclusion, we have demonstrated a special vdW heterostructure with 1D SWCNT and 2D MoS$_2$, which has shown superiority in nanoelectronics and nanooptoelectronics. Such a VPH not only facilely and effectively scales down the in-plane sizes of 2D material-based device into nanoscale by two cross-stacked metallic SWCNTs but also makes the

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crossed structure more applicable by introducing the 2D nanomaterials.[26] The VPH can be applied as high-performance FET, as it has high on/off ratio and high on current density at room temperature. The success in the CMOS demo further reveals the possibility of constructing complex logic circuits. The reduced in-plane size of the VPH also makes it expectable to apply the VPH in ultrahigh frequency electronics due to the reduced parasitic capacitive and inductive losses.[39] Moreover, the VPH device has potential in light detection, since it can map the Gaussian distribution of a focused laser beam. It can be further used to evaluate the quality of focused laser beams for laser lithography, confocal microscopy, and laser machining. More interestingly, a variety of VPH can be constructed for the big family of 1D and 2D materials, which is essential for the device design and applications.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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